CLAIM AMENDMENT

Please **AMEND** claim 40, as follows.

1-9. (Previously Withdrawn)

10. (Previously Amended) A contact structure of a wire, comprising:

a wire including a conductive material made of an aluminum-based material;

an inorganic insulating layer covering the wire and having a contact hole exposing the wire; and

a conductive layer made of indium zinc oxide, formed on the insulating layer and contacting the wire through the contact hole.

11. (Previously Amended) The contact structure of claim 10, wherein the contact hole has a shape including rounds or corner, and size of the contact hole is greater than 4 μm * 4 μm.

12. (Original) The contact structure of claim 10, wherein the inorganic insulating layer is made of silicon-nitride.

13. (Original) The contact structure of claim 10, wherein the wire has a flat surface.

14-39. (Previously Withdrawn)

40. (Currently Amended) A thin film transistor array panel, comprising:

a gate wire including a first conductive layer on an insulating substrate;

a gate insulating layer covering the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire including a second conductive layer on the gate insulating layer and the semiconductor layer;

a passivation layer covering the data wire; and

a transparent conductive layer pattern directly contacting with and connected to the gate wire through a first contact hole of the gate insulating layer or directly contacting with and connected to the data wire through the passivation layer,

wherein the first conductive layer ~~or~~ and the second conductive layer includes metal containing an aluminum-based material.

41. (Previously Cancelled)

42. (Previously Amended) The thin film transistor array panel of claim 40, wherein the surface of the metal containing the aluminum-based material is flat.

43. (Original) The thin film transistor array panel of claim 40, wherein the insulating layer and the passivation layer are made of silicon-nitride.

44. (Original) The thin film transistor array panel of claim 40, wherein the transparent conductive layer pattern is made of indium zinc oxide.

45. (Previously Amended) The thin film transistor array panel of claim 40, wherein the gate wire includes a gate line, a gate electrode connected to the gate line, and a gate pad which is connected to the gate line and receives a signal from an external circuit, and

the data wire includes a data line, a source electrode connected to the data line, a drain electrode separated from the source electrode and opposite to the source electrode with respect to the gate electrode, and a data pad that is connected to the data line and receives a signal from an external circuit.

46. (Previously Amended) The contact structure of claim 45, wherein the passivation layer further comprises a second contact hole exposing the data pad and a third contact hole exposing the gate pad along with the gate insulating layer,

the first to the third contact holes have a shape including rounds or corner, and size of the first to the third contact holes are greater than 4 μm * 4 μm.